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10/086,129	02/28/2002	David P. Schultz	X-1069 US	2232

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EXAMINER	
KERVEROS, JAMES C	

ART UNIT	PAPER NUMBER
2133	6

DATE MAILED: 06/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

RPG

Office Action Summary	Application No. 10/086,129	Applicant(s) SCHULTZ, DAVID P.	
	Examiner James C Kerveros	Art Unit 2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2, 5*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-27 are pending and are hereby presented for examination.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-27 are rejected under 35 U.S.C. 102(e) as being anticipated by Haroun et al. (US 6324662).

Regarding independent Claims 1, 11, Haroun discloses a method and a system for flexibly nesting JTAG TAP controllers (TAP 5) for intellectual property (IP) core (3) in an integrated circuit (1), as shown by a typical prior art testing system (FIG. 1), comprising:

A selectable bit register (Link shift register 406) in a host JTAG TAP controller (402) shown in FIG. 4 and also shown in FIG. 2 as a (TLM TAP0), comprising at least one available bit, as shown in FIG. 4.

A selector MUX 412 for selecting the available bit data signal (460) from (Link shift register 406), the selector extending an apparent length of an augmentation instruction shift register (AISR) 410 of the host JTAG TAP controller (402) by using the available bit from the selectable bit register (406), which is coupled with AISR 410 register through MUX 412 data signal 432 and MUX 416 data signal 456, FIG. 4.

Regarding independent Claims 7, 14, Haroun discloses a method and a system for flexibly nesting JTAG TAP controllers (TAP 5) for IP core (3) in an integrated circuit (1), as shown by a typical prior art testing system (FIG. 1), comprising:

A selector MUX 416 for choosing an IP core JTAG TAP controller (TAP1) from a plurality of JTAG TAP controllers (TAP1-4) corresponding to TDO1-TDO4 nested in the IP core subscriber and a multiplexer MUX 412 for programmably connecting the IP core JTAG TAP controller (TAP1) to a host JTAG TAP controller (402), shown in FIGS. 1, 2 and 4.

Regarding independent Claim 18, Haroun discloses a method comprising:

Forming instruction shift register (AISR) 410 for the IP (intellectual property) cores (3) FIG. 1, that are in series with the instruction registers (Link shift register 406) FIGS. 3 and 4.

Forming connections between (TLM TAP0) and IP Core JTAG logic (TAP1-4) of the IP core using a programmable interconnect MUX 412.

Emulating an instruction register (AISR) 410 of the IP core using a shift register (Link shift register 406) of the same length as the instruction register of the IP core.

Regarding independent Claim 21, Haroun discloses a system for performing boundary scan functions on a plurality of IP cores (3) in an integrated circuit (1), FIG. 1, comprising:

An FPGA-based system-on-chip (SoC), such as IP core (3) in the integrated circuit (1), as shown by a typical prior art testing system (FIG. 1), comprising a plurality of IP cores (3) each including a JTAG TAP controller (5) and a host JTAG (TAP0) controller coupled to each of the first JTAG (TAP1-4) controllers, FIGS. 1 and 2.

Regarding Claims 2, 12, Haroun discloses a selector MUX 416 for choosing an IP core JTAG TAP controller (TAP1) from a plurality of JTAG TAP controllers (TAP1-4) corresponding to TDO1-TDO4 nested in the IP core subscriber and a multiplexer MUX 412 for programmably connecting the IP core JTAG TAP controller (TAP1) to a host JTAG TAP controller (402), shown in FIGS. 1, 2 and 4.

Regarding Claim 3, Haroun discloses emulating the instruction register (AISR) 410 of the IP core using a shift register (Link shift register 406) before programmable configuration of the IP (intellectual property) core (3), FIG. 1.

Regarding Claims 4, 10, 13, 17, Haroun discloses a shift circuit (Link shift register 406) for shifting TDI instruction corresponding to the selected IP core JTAG TAP controller (TAP1) through instruction shift register (AISR) 410 and causing the controller (TAP1) to execute the instruction in the shift register (AISR) 410.

Regarding Claims 5, 6, Haroun discloses manually and programmably selecting through MUX 412 the available bit from the selectable bit register (Link shift register 406), FIG. 4.

Regarding Claims 8, 9, 15, 16, Haroun discloses a selectable bit register (Link shift register 406) in a host JTAG TAP controller (402) shown in FIG. 4 and also shown in FIG. 2 as a (TLM TAP0), comprising at least one available bit from, as shown in FIG. 4 and wherein the (Link shift register 406) extends an apparent length of the augmentation instruction shift register (AISR) 410 of the host JTAG TAP controller (402) by using the available bit from the selectable bit register (406), including a combined length of the bit from the (Link shift register 406) and the bits comprising the instruction register (406).

Regarding Claim 19, Haroun discloses selectably accessing the nested JTAG TAP controllers (TAP1-TAP4) of the IP cores via a programmable input/output (Tap Linking Module, TLM), FIG. 2.

Regarding Claim 20, Haroun discloses emulating instruction register (AISR) 410 of the IP core using a shift register (Link shift register 406) including selectably varying the size of the shift register, using shift enable signals 452, based on the number of IP cores in a given configuration of the integrated circuit (1). In the summary of the invention, Haroun further describes the instruction scan operation mode of the TAP, where instruction data is scanned through both the connected TAP and an augmentation instruction shift register (AISR) within the TLM. The TLM's AISR extend the instruction register length of the connected TAP by the number of the bits within the AISR.

Regarding Claims 22, 23 Haroun discloses integrated circuit (1) including a host JTAG TAP controller (402) shown in FIG. 4 and also shown in FIG. 2 as a (TLM TAP0)

and further including a selector circuit MUX 416 coupled between the first JTAG (TAP1-4) controllers and the host JTAG TAP controller (TLM TAP0).

Regarding Claim 24, Haroun discloses integrated circuit (1) includes a host JTAG TAP controller (TLM TAP0) and the selector circuit MUX 416.

Regarding Claim 25, Haroun discloses a host JTAG TAP controller comprising:

A selectable bit register (Link shift register 406) coupled to the selector circuit MUX 416 through data signal 432 and providing a selected bit at (460).

An instruction register (AISR) 410 coupled to the selectable bit register (460), the instruction register having an output (433) providing an instruction to TLM 404, having an apparently extended length combined with the bits shifted from the output of the (Link shift register 406), FIG. 4.

Regarding Claims 26, 27, Haroun discloses a selector circuit, such as programmable input/output (Tap Linking Module, TLM) FIG. 2, coupled between the nested JTAG TAP controllers (TAP1-TAP4) of the IP cores and the host JTAG (TAP0) controller.

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James C Kerveros whose telephone number is (703) 305-1081. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

U.S. PATENT OFFICE
Examiner's Fax: (703) 746-4461
Email: james.kerveros@uspto.gov

Date: 18 June 2004
Office Action: Non-Final Rejection

By: _____

James C Kerveros
Examiner
Art Unit 2133

Greg J. Lamarre
for

Albert DeCady
Primary Examiner